```
VERSUCH5b

;PALASM Design Description
;---------------------------------- Declaration Segment ------------
TITLE Versuch5 - Teil b
PATTERN
REVISION
AUTHOR ???
COMPANY RWTH
DATE 22/06/04
CHIP _teilb PALCE16V8
;---------------------------------- PIN Declarations ---------------
PIN 1 clk
PIN 2 DA
PIN 3 DB
PIN 4 DC
PIN 5 DD
PIN 6 ENP
PIN 8 LOAD
PIN 10 GND
PIN 11 OE
PIN 12 QA REGISTERED
PIN 13 QB REGISTERED
PIN 14 QC REGISTERED
PIN 15 QD REGISTERED
PIN 16 RCO COMBINATORIAL
PIN 20 Vcc
;---------------------------------- Boolean Equation Segment ------
EQUATIONS
RCO = (ENP * QA * /QB * /QC * QD * LOAD);
QA = ( /LOAD*DA)+(LOAD*QA*/ENP) + ENP*(/QA*LOAD)

QB = ( /LOAD*DB)+(LOAD*QB*/ENP) + ENP*((QA*/QB*/QC*/QD*LOAD)+
(/QA*QB*/QC*/QD*LOAD)+(QA*/QB*QC*/QD*LOAD)+(/QA*QB*QC*/QD*LOAD))

QC = ( /LOAD*DC)+(LOAD*QC*/ENP) + ENP*((QA*QB*/QC*/QD*LOAD)+
(/QA*/QB*Qc*/QD*LOAD)+(QA*/QB*QC*/QD*LOAD)+(/QA*QB*QC*/QD*LOAD))

QD = ( /LOAD*DD)+(LOAD*QD*/ENP) + ENP*((QA*QB*QC*/QD*LOAD)+
(/QA*/QB*/QC*QD+LOAD))
;---------------------------------- Simulation Segment ------------
SIMULATION
SETF /LOAD /DA /DB /DC /DD /ENP /OE
clockf clk
SETF ENP LOAD
for i:= 1 to 10 do
begin
clockf clk
end
;-------------------------------------------------------------------
```